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SUGGESTIONS FOR IMPROVEMENTS OF TIMING CIRCUITS WITH TUNNEL DIODES†

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In this letter we will show how the results carried out in our paper[1]) should be applied straight to calculate the "slewing time" of a zero crosser circuit using a tunnel diode.

A short analysis of a circuit[2]) published in 1963, is made in order to suggest some improvements for the timing techniques. This circuit attains in a very simple way the appreciable result to give a variable threshold with little slewing in timing information. A tunnel diode monostable discriminator is associated with a synchroniser starting at zero cross of the bipolar pulse obtained from the input pulse differentiation. The idea has been applied once more in recent works[illegible]) with satisfaction.

Our analysis is completely devoted to the synchronising circuit appearing in [2]). Furthermore, we give the logic scheme of a circuit under development with which we hope to improve the performance of timing.

The *analysis of the timing circuits*[2-6]) about which we will publish more complete results later, has suggested us three essential conditions to be satisfied to actuate a tunnel diode with good time performances. These are:

1. to lower as much as possible the zero crosser threshold;
2. to select the input pulse dynamics so, that the minimum selected amplitude must be very much higher than the threshold of the zero crossing detector;
3. to limit the input pulse after the zero in order to obtain the switching of the tunnel diode during a time independent from the input pulse overdrive.

The circuits we have analysed follow different techniques, but generally they satisfy the three conditions above mentioned.

The circuit in [2]) is a zero crossing detector utilizing a tunnel diode discriminator biased as a bistable on its high voltage state. A back-diode acts as a limiter of the input pulse after the zero. The input dynamics selection is accomplished by the hysteresis of the tunnel diode zero crosser; then the selected pulses are able to switch the tunnel diode at the peak when the zero is crossed so that the circuit has a very sensitive actual threshold. Evidently, the slewing time depends on how much near the peak the zero is crossed when the amplitude of the pulses vary before the zero point.

Now, at first, let us calculate the actual hysteresis of the circuit when the biasing point is $j_0 = 1$* on the high voltage state. It is the value of the dynamic threshold of a tunnel diode Schmidt discriminator with zero bias, with a peak current equal to the difference between the bias and valley current $j^*_p = 1 - j_v$, and the peak voltage equal to the difference between the forward peak projected voltage and the valley voltage $v^*_p = v_{fp} - v_v$.

We can assume this circuit (only to evaluate its threshold) to be equivalent to a tunnel diode mono-

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* We refer the current and voltage values to the peak point values I_p, V_p, that is: $j = I/I_p$ and $v = V/V_p$. Then we define[1]):

$$K = L/(R_p^2 C); \quad R_p = V_p/I_p; \quad \tau = t/(R_p C),$$

where L is the buffer inductance of a monostable circuit and C is the capacitance of the tunnel diode at the valley point.

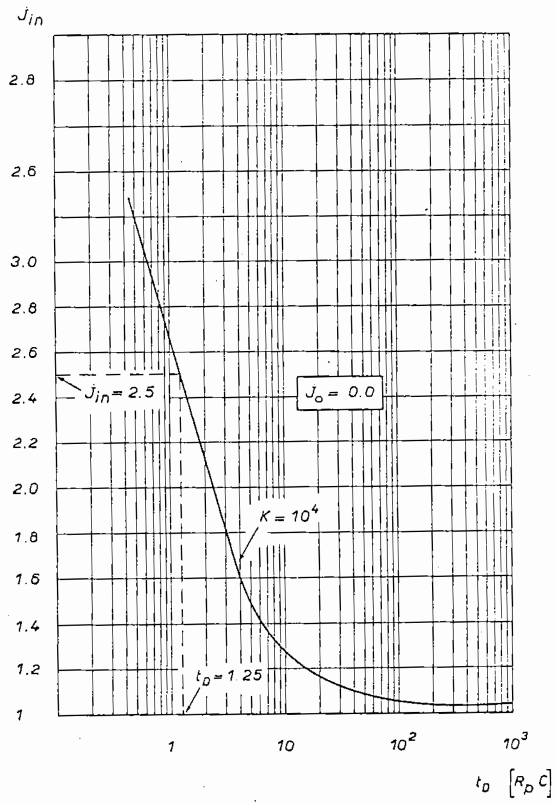

Fig. 1. Threshold vs time delay for ramp input.

stable circuit very light loaded ($K = 10^4$) in order to utilize the results in [1]).

In fig. 1, extracted from [1]), the normalized threshold current vs switching time (normalized to $R_p C$) is reported for ramp input pulses.

Referring to the tunnel diode (1 N 2969), utilized in [2]), we have:

$$j_p^* \simeq 0.87; \quad v_p^* \simeq 2.3; \quad R_p \simeq 30\,\Omega;$$
$$R_p^* = (v_p^*/j_p^*)R_p \simeq 80\,\Omega; \quad R_p^* C \simeq 2\,\text{ns}.$$

For a standard triggering pulse of rise-time $t_r = 2.5$ ns, ref. [2]), from fig. 1 we obtain for $t_D = t_r/(R^*{}_p C) = 1.25$ a dynamic threshold of:

$$j_{in} \simeq 2.5 \text{ and then } I_{in} \simeq 4.8 \text{ mA}.$$

The minimum amplitude discrimination is reported in [2]) to be 7 mA; this is because the biasing point is $j_0 > 1$.

More precisely, if we take the hysteresis $h = 7/I_p$ (mA) we obtain j_0 from $h = j_{in}(j_0 - j_v)$ and then $j_0 \simeq 1.4$.

Let us now calculate the minimum slewing time for an input dynamics selected by the calculated hysteresis.

Supported by experimental results in progress, we assume that the work point is at $j = 1$ on the low voltage state of the tunnel diode for the lower amplitude selected when the zero is crossed and not at $j = 1.4$. This is due to the intrinsic delay of the tunnel diode. Therefore, the delay between the zero crossing instant and the time at the regenerative point of the tunnel diode is zero for these input pulses.

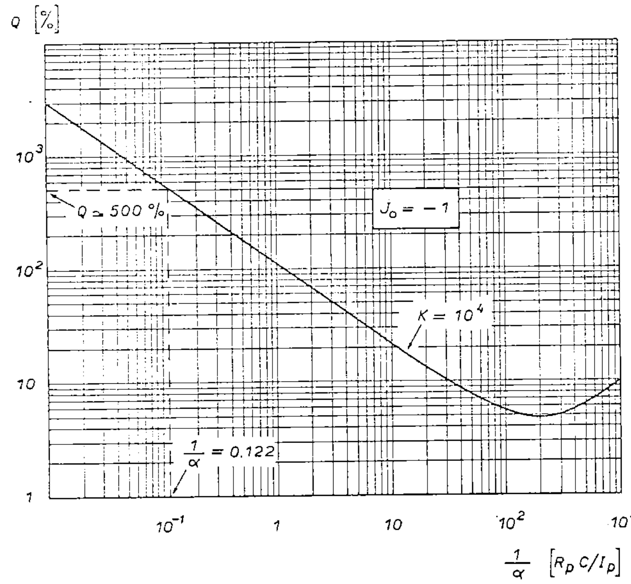

Fig. 2. Threshold vs $1/\alpha$ for ramp input.

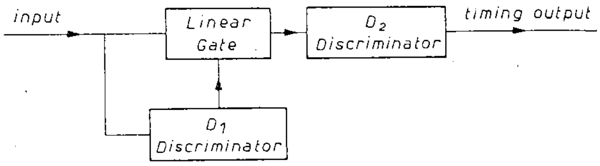

Fig. 3. Logic scheme for timing system.

Moreover we assume that the work point at the zero cross is at $j = -1$ for the higher amplitude of the input pulses (60 mA). In fig. 2 we have reported the threshold $[Q = 100\,(j_{in} + j_0 - 1)]$ vs $1/\alpha$ ($\alpha = j_{in}/\tau$) for ramp input and bias current $j_0 = -1$. We obtain for $1/\alpha = 0.122$, $Q = 500\%$ and then

$$j_{in} = 7; \quad \tau = j_{in}/\alpha \simeq 0.85; \quad t = 0.85 R_p C = 0.65 \text{ nsec.}$$

This is the minimum slewing time obtainable: in fact we have not considered the delays introduced by different switching times caused by different overdrives.

The conditions cited above and satisfied for good timing with tunnel diodes bring straight to the logic scheme shown in fig. 3.

If threshold S_1 of discriminator D_1 is higher than threshold S_2 of discriminator D_2, the input signal that will fire D_2 will be higher than its threshold, and than a good timing action may be performed. We require only that the timing information of the input must be kept at the AND gate.

We will point out that the proposed scheme refers only to the synchronizer.

If one wants to perform also an amplitude analysis, the threshold of D_1 must be varied at the condition that $S_1 \gg S_2$.

An actual circuit may be obtained following a scheme that respects the logic functions of the one in fig. 3. This will be done to simplify the practical realisation of the circuit.

On the basis of this analysis the development of a circuit is in progress.

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